File No: 3552/0K204

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kunihiko SUZUKI; Changming ZHOU

Serial No: TBA (U.S. National Phase of PCT/JP01/04032, filed May 15, 2001)

Filed: Concurrently Herewith

For: **MATCHED FILTER CIRCUIT**

PRELIMINARY AMENDMENT

Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Attn.: Box PCT, RO/US

Sir:

Prior to examination, Applicants wish to amend the above-identified application as follows.

IN THE SPECIFICATION

Following the title, please add the following paragraph:

This application is a 371 of International Application No. PCT/JP01/04032 filed May 15, 2001, which was not published in English and which claims benefit of Japanese Patent Application No. 2000-143925 filed on May 16, 2000.

IN THE CLAIMS

Please amend claims 4 and 6 to read as follows:

4. (Amended) The matched filter circuit according to claim 2, characterized in that each of the hold circuit groups includes:

m switches, each connected with the output of the first sum and product arithmetic unit in parallel and sequentially outputting each of m outputs;

hold circuits, each connected to an output of each switch and holding an output of each switch; and

a multiplexer selectively outputting any one of the outputs of the hold circuits.

6. (Amended) The matched filter circuit according to claim 3, characterized in that each of the hold circuit groups is a memory circuit, and read/write of the memory circuit is carried out in a manner that in $m \times n$ cycles, read and write are alternately carried out in m periods, and in $m \times (n-1)$ periods other than above, only read is carried out.

REMARKS

Entry of these amendments, prior to examination, is respectfully requested.

The application has been amended to claim benefit of a prior filed copending international application designating the United States of America, which application claims benefit of a prior filed Japanese patent application.

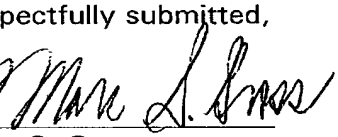
The claims are amended for the purpose of eliminating multiple claim dependencies.

A marked-up version of the claims, which indicates all amendments made, is submitted herewith.

None of the amendments introduce new matter.

An early and favorable examination is earnestly solicited.

Respectfully submitted,



Date: January 16, 2002

Marc S. Gross
Reg. No. 19,614
Attorney for Applicants

DARBY & DARBY P.C.
805 Third Avenue
New York, NY 10022
212-527-7700

EXPRESS MAIL CERTIFICATE
Date 1/16/02 Label No. EL767722596US
I hereby certify that, on the date indicated this paper or fee was deposited with the U.S. Postal Service and that it was addressed for delivery to the Assistant Commissioner of Patents & Trademarks, Washington, DC 20231 by "Express Mail Post Office to Addressee" service.
D BECK
Name (Print) Signature

File No: 3552/0K204

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kunihiko SUZUKI; Changming ZHOU

Serial No: TBA (U.S. National Phase of PCT/JP01/04032, filed May 15, 2001)

Filed: Concurrently Herewith

For: **MATCHED FILTER CIRCUIT**

MARK UP TO PRELIMINARY AMENDMENT

Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Attn.: Box PCT, RO/US

Sir:

Prior to examination, Applicants wish to amend the above-identified application as follows.

IN THE SPECIFICATION

Following the title, please add the following paragraph:

This application is a 371 of International Application No. PCT/JP01/04032 filed May 15, 2001, which was not published in English and which claims benefit of Japanese Patent Application No. 2000-143925 filed on May 16, 2000.

IN THE CLAIMS

Please amend claims 4 and 6 to read as follows:

4. (Amended) The matched filter circuit according to claim 2 [or 3], characterized in that each of the hold circuit groups includes:

m switches, each connected with the output of the first sum and product arithmetic unit in parallel and sequentially outputting each of m outputs;

hold circuits, each connected to an output of each switch and holding an output of each switch; and

a multiplexer selectively outputting any one of the outputs of the hold circuits.

6. (Amended) The matched filter circuit according to claim 3 [or 4], characterized in that each of the hold circuit groups is a memory circuit, and read/write of the memory circuit is carried out in a manner that in $m \times n$ cycles, read and write are alternately carried out in m periods, and in $m \times (n-1)$ periods other than above, only read is carried out.